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Multi-channel UART with auto baud rate detection

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Abstract:
This project is about the design and implementation of a Multi-channel UART with automatic baud rate detection. To meet modern complex control systems communication demands, the project presents a multi-channel UART controller based on FIFO (First In First Out) technique and FPGA technology (Field Programmable Gate Array).
It is designed with FIFO circuit block and UART (Universal Asynchronous Receiver Transmitter) circuit block within FPGA to implement communication in modern complex control systems quickly and effectively.
This controller can be used to implement communication when master equipment and slave equipment are set at different baud rate. It also can be used to reduce synchronization error between sub-systems in a system with several sub-systems. The controller is reconfigurable and scalable.
Now a days electronic systems are getting complicated wherever it's used e.g. home, automobile, aerospace etc. Most of the peripherals is having UART interface e.g Camera, Bluetooth device, Wi-Fi device etc. Most of the time we have limited UART port on board mainly 2 or 3 that limits the capability of the system.
Through this proposed system, we can configure N no of UART channel with flexible baud rate. Most of the peripheral requires a variable baud rate system as per speed requirement but mostly baud rate of UART can't be changed at run time.
Through this system, we have automatic baud rate detection and hence it is possible to switch between different baud rates.
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Keywords: Multi-channel UART with auto baud rate detection, UART, FIFO, FPGA, Wi-Fi.

1. INTRODUCTION

1.1 UART

A UART (Universal Asynchronous Receiver/Transmitter) is the microchip with programming that controls a computer's interface to its attached serial devices.
Specifically, it provides the computer with the RS-232C Data Terminal Equipment (DTE) interface so that it can "talk" to and exchange data with modems and other serial devices. As part of this interface, the UART also Converts the bytes it receives from the computer along parallel circuits into a single serial bit stream for outbound transmission On inbound transmission, converts the serial bit stream into the bytes that the computer handles adds a parity bit (if it's been selected) on outbound transmissions and checks the parity of incoming bytes (if selected) and discards the parity bit adds start and stop delineators on outbound and strips them from inbound transmissions. Handles interrupts from the keyboard and mouse (which are serial devices with special ports) .May handle other kinds of interrupt and device management that require coordinating the computer's speed of operation with device speed serial transmission is commonly used with modems and for non-networked

UART is a device that has the capability to both receive and transmit serial data. UART exchanges text data in an American Standard Code for Information Interchange (ASCII) format in which each alphabetical character is encoded by 7 bits and transmitted as 8 data bits. For transmission the UART protocol wraps this 8 bit sub word with a start bit in the least significant bit (LSB) and a stop bit in the most significant bit (MSB) resulting in a 10 bit word format. a reset and attempts to obtain the satellite signals and calculates a new position.

FIFO

FIFO, or First In, First Out, is a method that relates to the organization and manipulation of data according to time and prioritization. In essence, the queue processing technique is done as per a first-come, first-served behavior. The algorithm of the operating system scheduling gives every process CPU time according to the order it comes. Each item is stored in a queue data structure. The first data, which is added to the queue, will be the first data to be removed. Processing continues to proceed sequentially in this same order. FIFO is used for

synchronization purposes in computer and CPU hardware. FIFO is generally implemented as a circular queue, and thus has a read pointer and a write pointer. A synchronous FIFO uses the same clock for reading and writing. An asynchronous FIFO, however, uses separate clocks for reading and writing.

The keyboard buffer is an example of a FIFO memory. In the FIFO scheme, data is not accessed randomly from any location as in RAM and ROM memories where any location can be accessed by specifying the location address. In the FIFO memory the data which is written into the memory first is the first one to be read out. As mentioned above, FIFO memories are used to connect two digital devices that produce and consume data at different rates. Assuming that Device A produces data at a certain rate and device B consumes the data at a different rate. A FIFO memory is connected between the output of device A and the input of device B, the data produced by device Ais written into the FIFO memory.

2. RELATED WORK

The UART is the use of the serial communication protocol, which permits the full duplex communication in serial link. They design the hardware implementation of a high speed & competent UART using Field Programmable Gate Array. The UART consists of three components, receiver, transmitter & baud rate generator which is also frequency divider. They simulated on Modelsim SE 10.0a and design by using Verilog description language which has been synthesized on FPGA kits like as Spartan3 & Virtex4. After analyzing the comparative analysis conclude that there is a difference in between the number of slices, LUTs and the maximum frequency. The results are quite stable and reliable and have great flexibility with high integration. If we use FIFO in making the UART our design becomes more flexible, stable and reliable which provides highest bps rate [1]. A UART is a full duplex receiver and transmitter. It is the chip with programming that controls a computer's an interface to its connected serial devices. It manages the transmission between serial and parallel data. The whole process of serial transmission is operating on the principle of the shift register. In data transmission through the UART.

Once the baud-rate has been originated, both the transmitter & the receiver's internal clock are set to the identical frequency. [2] Tenure is concerned, developing a serial communication protocol including bit synchronization, automatic baud rate detection with selection and bus, frequency division according to the input clock. All modules are simulated on Xilinx ise [3]. Their work presents design method of asynchronous FIFO and structure of controller. This controller is designed with FIFO circuit block and UART (universal asynchronous receiver transmitter) circuit block with in FPGA to implement communication in modern complex control systems quickly and e.

ffectively. This controller can be used to implement communication when master equipment and slaver equipment are set at different baud rate[7]. It can also be used to reduce synchronization error between sub systems in a system with several sub systems. The controller is reconfigurable and scalable. Problem with large area.[4] This work proposes an integrated architecture for a UART module to be used with MIMO-OFDM hardware platform, the purpose of this module is to enable the communication between Matlab and FPGA board. Problem with design complexity [5].

A Universal Asynchronous Receive/Transmit (UART) with BIST capability has the objectives of testing the UART on chip itself and no external devices are required to perform the test[4]. This paper focuses on the VHDL implementation of UART with embedded BIST capability using FPGA technology. The paper presents the architecture of UART with BILBO which tests the UART for its correct ability. The whole design is synthesized and verified using Xilinx ISE Simulator and Modelsim Simulator. Dr. T.V.S.P.Gupta et. al. [3] The simulated waveforms presented in this paper have proven the reliability of the VHDL implementation to describe the characteristics and the architecture of the designed UART with embedded BIST[8]. The simulated waveforms also have shown the observer how long the test result can be achieved by using the BIST technique. With the implementation of BIST, expensive tester requirements and testing procedures starting from circuit or logic level to field level testing are minimized[10]. The LFSR replaces the function of the external tester features such as a test pattern generator by automatically generating pseudo random patterns to give 100% fault coverage to the UART module[11]. The MISR acts as a compression tool, compressing the output result when automatic pseudo random pattern is fed to the UART.

3.Methodology

The below diagram gives a pictorial representation of the system.

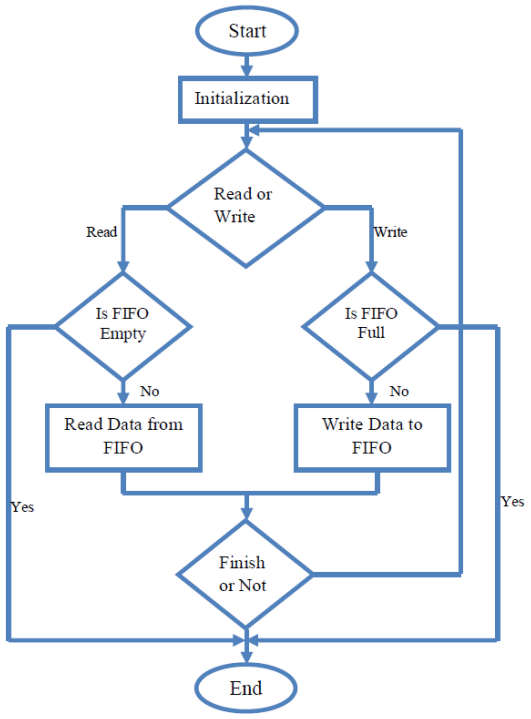

Fig. 1 Proposed system.

The idea is to create a multi channel UART with capability to detect baud rate automatically. In the multi-channel controller, there are different blocks including UART block, Status Detectors, asynchronous FIFOs block and Baud Rate Generator block. Each block has different function in the controller. The first part is UART circuit block. It consists of three parts Receive Circuit, Transmit Circuit and Control/Status Registers. The Transmit Circuit consists of a Transmit Buffer and a Shift Register. Transmit Buffer loads data being transmitted from local CPU. Shift Register accepts data from the Transmit Buffer and send it to the TXD pin one by one bit. The Receive Circuit consists of a Receive Shift Register and a Receive Buffer. The Receive Shift Register receives data from RXD one by one bit. The Receive Buffer loads data from long-distance MCU and gets it ready for the local PC to read. The Control Register a special function register is used to control the UART and indicate status of it. According to each bit's value the UART will choose different kind of communication method and the UART knows what to do to receive or transmit data. FIFOs are used to store data received from the PC and get ready for sub MCUs. When writing data into FIFOs and reading data out of FIFOs we could set different clock domains according to the PC's and MCUs' Baud Rate. So it can be used to implement communications between MCUs.

3.2 Software Required

Software: Xilinx ISE 10.
Language: VHDL

4. PRACTICAL MODEL

UART transmitter and receiver codes in VHDL is developed and tested through test bench.

4.1 Results

4.1.1 Simulation Result of UART Test

Test Case #1: Reset

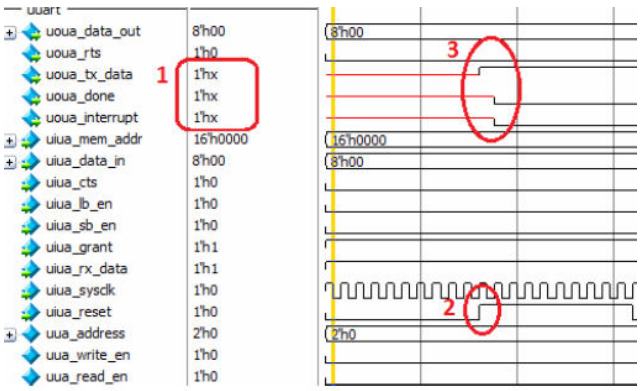

Figure 2: Simulation reset

1. Before the reset signal is asserted, the signals are in unknown state.
2. Reset signal asserted.
3. All output signals are set to a default state.

Test Case #2: Send data with Even Parity

1. Data input to be written to configuration register.
2. Data input is written to configuration register. Enable parity (bit 3) is asserted
and parity bit (bit 4) is de-asserted.
3. Data input to be transmit to external side.

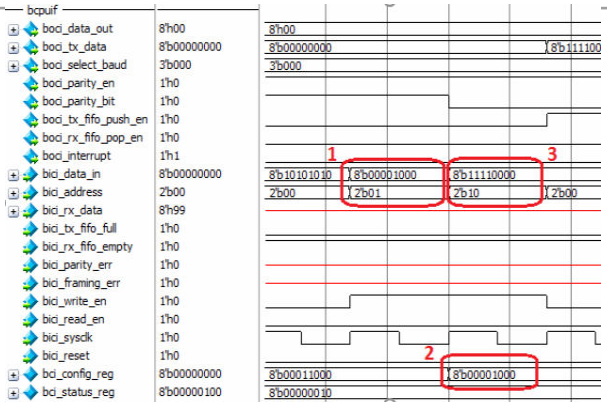

Figure 3: Send data with even parity

5Conclusions

From result of proposed work it is concluded that the design uses VHDL/Verilog language to acquire the modules of universal asynchronous receiver transmitter. By Using the Xilinx software to complete simulation. The results are stable and reliable according to binary information. The outcome is feasible and efficient with power reduction and also area reduction. Especially in the field off electronic design technology has recently become widely used, this design shows great significance and can be used in various applications.

5.1 Future perspective of Work

- The system provides huge chance of expansion.
- Error handling mechanism for channels can be implemented.
- Run time check for baud rate stabilization can be done.
- The system will provide channel expansion at run time.
- In system has potential in expansion of use in different industries for real time embedded systems products.

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