

Adaptive Filter Design using LMS Algorithm and Sigma Delta Modulation

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Abstract: This paper presents the implementation and design of adaptive noise cancelling filters using the hybrid LMS and Sigma Delta Modulation approach. It has been clearly shown how the process of Sigma Delta Conversion used in ADCs can achieve higher speeds even after employing Oversampling above Nyquist rate with the LMS algorithm. The various parameters affecting the design and performance of the Delta Sigma employed filter design have been analyzed. Stability considerations of higher order sigma delta modulators have also been analyzed to attain an optimized approach to decide upon the design of the SDM. Variation in the SNR has been shown with changes in Over Sampling Rate.

Keywords: Adaptive Filter Design, Sigma delta modulator, LMS Algorithm, Over Sampling Rate, Signal to Noise Ratio, Dynamic Range, Quantization Noise.

INTRODUCTION

Adaptive filter design finds its applications in several fields of signal processing such as speech processing, analog to digital conversion, image processing etc. The very essence of adaptive filtering rests on the principle that the noise conditions faced by signals can vary. Adaptive filter adjust their coefficients to minimize an error signal and can be realized as finite

impulse response (FIR), infinite impulse response (IIR), lattice and transform domain filter. Although real world signals are analog, it is often desirable to convert them into the digital domain using an analog to digital converter (ADC). Signal processing in the digital domain is useful in digital storage, biomedical applications, and industrial applications - from instrumentation to communication. Sigma Delta Modulators achieve a high degree of insensitivity to analog circuit imperfections, thus making them a good choice to realize embedded analog-to-digital interfaces. Application based and sophisticated design techniques demand Radio Frequency Identification Techniques which find its application in object tracking, etc. Sigma Delta ADC is high resolution ADC and acts as a major building block in RFID applications. [1] As per the sampling frequency, ADC is classified into two categories: Nyquist ADCs and Sigma- Delta ADCs. Nyquist ADCs have a lower effective number of bits due to process variation and mismatching [2]. One technique, Sigma Delta modulation, which is based on the combination of oversampling and quantization error shaping techniques, has become quite popular for achieving high resolution and high accuracy. [3] One significant advantage of the method is that analog signals are converted using only a 1-bit ADC and analog signal processing circuits having a precision that is usually much less than the resolution of the overall converter. Using sigma-delta A/D methods, high resolution can be obtained for only a low to medium signal bandwidths. The Oversampling behavior of the Sigma Delta Modulator restricts the

bandwidth which can be overcome by using higher order architecture.

The Signal to Noise Ratio of Sigma Delta Modulator is dependent upon the number of bits of quantizer and is independent of amplitude of input signal. The N - bit quantizer has 2 levels and separated by V LSB. The amplitude of full scale sine wave input is $2^{N-1} V$ LSB. Peak to peak value is given by $2^N V$ LSB Mean Square Value of the Signal is given by:

$$S = (2^{N-1} V_{\text{LSB}})^2 / 2$$

Mean squared Noise is given by the expression:

$$N = V_{\text{LSB}}^2 / 12$$

Therefore,

Signal to Noise Ratio (SNR) is given by:

$$[(2^{N-1} V_{\text{LSB}})^2 / 2] / [V_{\text{LSB}}^2 / 12]$$

which reduces into

$$\text{SNR} = 12^{2N}$$

Also,

$$\text{SNR} = 6.02N + 1.76 \text{dB}$$

SYSTEM DESIGN

The proposed system design is given by:

Firstly, initial parameters are defined like Over Sampling Ratio and Number of Quantization bits. In the next step, as per the order of Sigma Delta Modulator, loop filter parameters i.e. Signal Transfer Function and Noise Transfer Function are designed. Then input signal is defined for simulation of Sigma Delta Modulator through which performance parameters like Signal to Noise Ratio and Effective Number of bits are calculated. The stability of Sigma Delta Modulator depends upon loop filter parameter, and input signal amplitude. So, for designing a stable Sigma Delta Modulator, these parameters are considered.

The transfer function $Lo(z)$ and $Li(z)$ can also be realized by using feed forward signal paths to create the zeros of the NTF.

The transfer function of the feedback filter is

$$L_1(z) = -a_1 I(z) - a_2 I(z)^2 - \dots - a_n I(z)^n$$

Where $I(z)$ is the delaying integrator's transfer function. The signal filter function is

$$L_0(z) = b_1 (a_1 I + \dots + a_n I^n) + b_2 (a_2 I + \dots + a_n I^{n-1}) + b_{n+1}$$

Considering $b_2 = b_3 = \dots = b_n = 0$ and $b_1 = b_{n+1} = 1$

Therefore, $L_0(z) = 1 - L_1(z)$ and $STF = 1$,

We get and provides $STF = 1$.

The error computation based filter design using the LMS approach is implemented using the relation:

$$\min E[z^2] = E[s^2] + \min E[(n_0 - y)^2]$$

The flowchart of the proposed system is shown below:

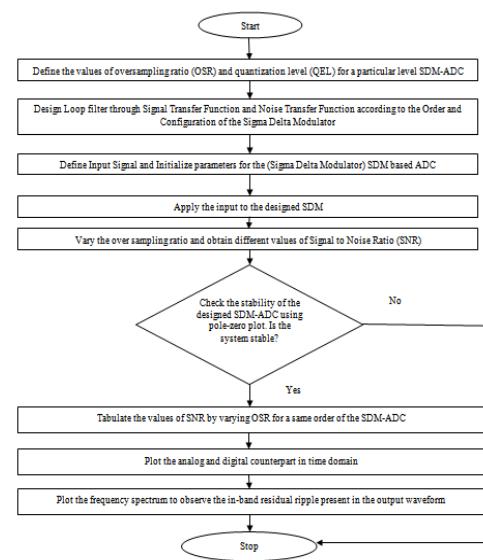


Fig.1: Flow Chart for Proposed System

RESULTS

This section will deal with the comparative analysis of fourth order Sigma Delta Modulator with respect to different topologies for parameters like signal to noise ratio and effective number of bits. For realization initial parameters are taken for all topologies as OSR = 4, out of band gain (OBG) = 1.5, Quantization Level=7. A comparison of different parameters is done for different values of OSR. For the CIBF topology, Figure 5.12 gives the Realization of STF and NTF in voltage, Figure 5.13 shows the Realization of STF and NTF in dB, Figure 5.14 shows the time domain simulation of fourth order Sigma Delta Modulator , Figure 5.15 shows the integrator states of fourth order Sigma Delta Modulator where x_1 is the output of first integrator, x_2 is the output of second integrator, x_3 is the output of third integrator, x_4 is the output of fourth integrator and Figure 5.16 shows the frequency domain simulation of fourth order Sigma Delta Modulator.

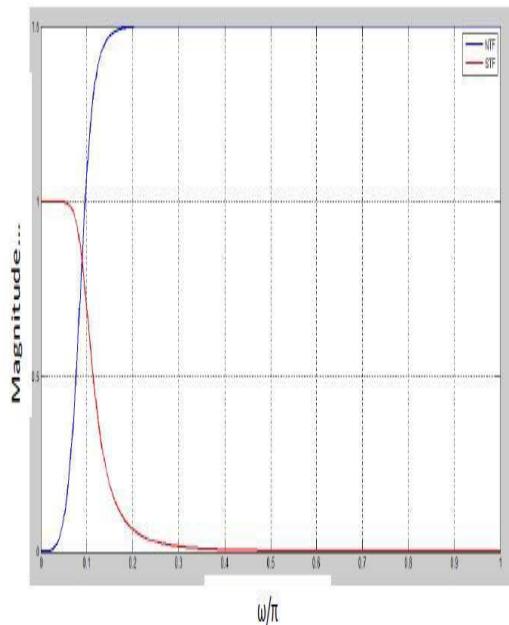


Fig.2 Realization of STF and NTF in voltage

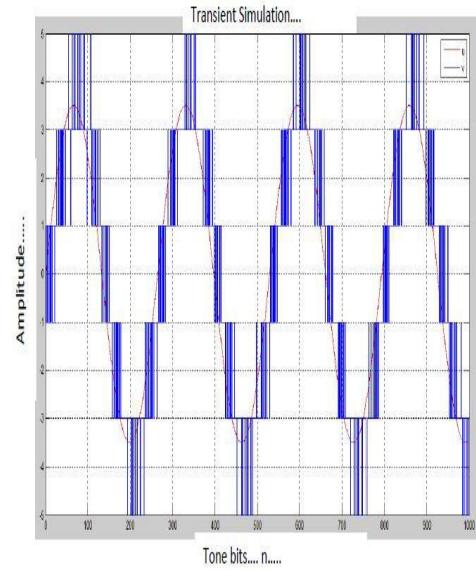


Fig.3 Time Domain Simulation Of Fourth Order Sigma Delta Modulator With CIBF Architecture

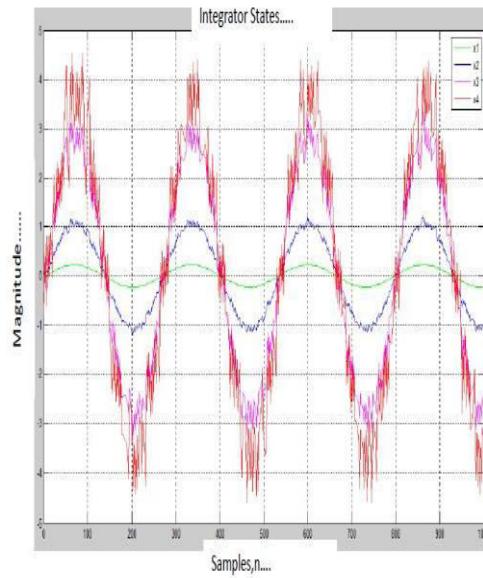


Fig.4 Integrator States Of Fourth Order Sigma Delta Modulator With CIBF Architecture

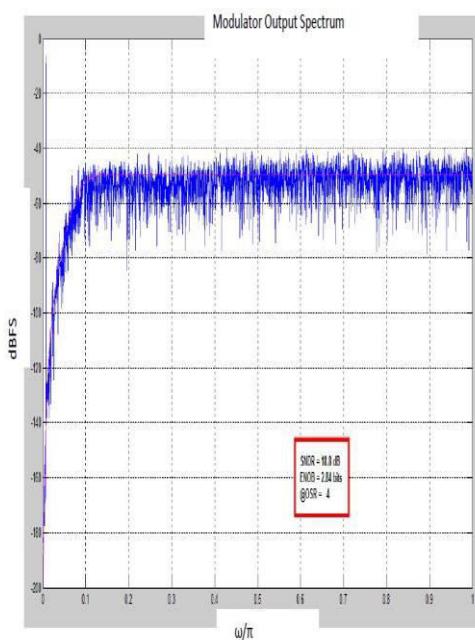


Fig.5 Frequency Domain Simulation Of Fourth Order Sigma Delta Modulator With CIBF Architecture

| Sr. No. | OSR | SNR | ENoB |
|---------|-----|-------|-------|
| 1 | 2 | 14.1 | 2.04 |
| 2 | 4 | 18.8 | 2.84 |
| 3 | 8 | 25.7 | 3.98 |
| 4 | 16 | 47.1 | 7.53 |
| 5 | 32 | 74.3 | 12.05 |
| 6 | 64 | 103.6 | 16.92 |
| 7 | 128 | 137.4 | 22.53 |

Table.1 Analysis Of Fourth Order Sigma Delta Modulator For Signal To Noise Ratio And Effective Number Of Bits.

Thus the aforesaid discussions along with the relevant waveforms and tables are self explanatory for the performance of higher order sigma delta modulators. The above comparative analysis concludes that parameters affecting the performance of Sigma Delta Modulator like Signal to Noise Ratio

and Effective Number of Bits increases with increase in Over Sampling Ratio. Also, with the increase in order of modulator and quantization level, high SNR can be achieved at low OSR value. But with the increase of order, the modulator becomes unstable and also, maximum usable input signal amplitude decreases.

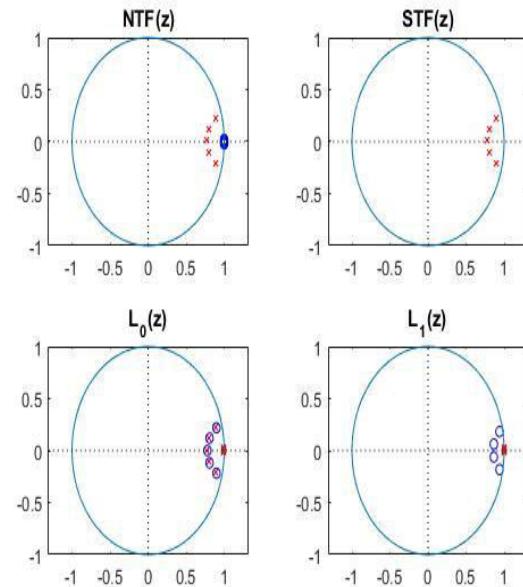


Fig.6 Stability Analysis of 5th Order Filter

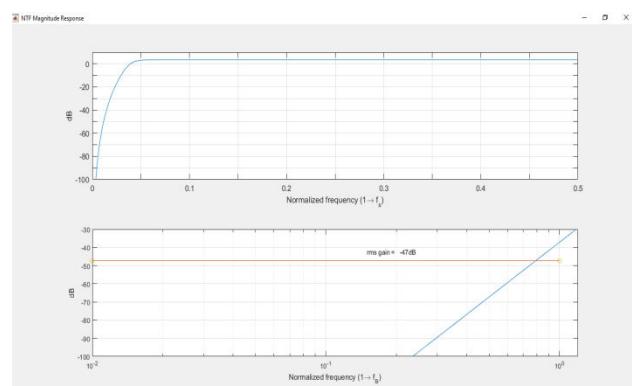


Fig.7 Stability Analysis of 5th Order Filter

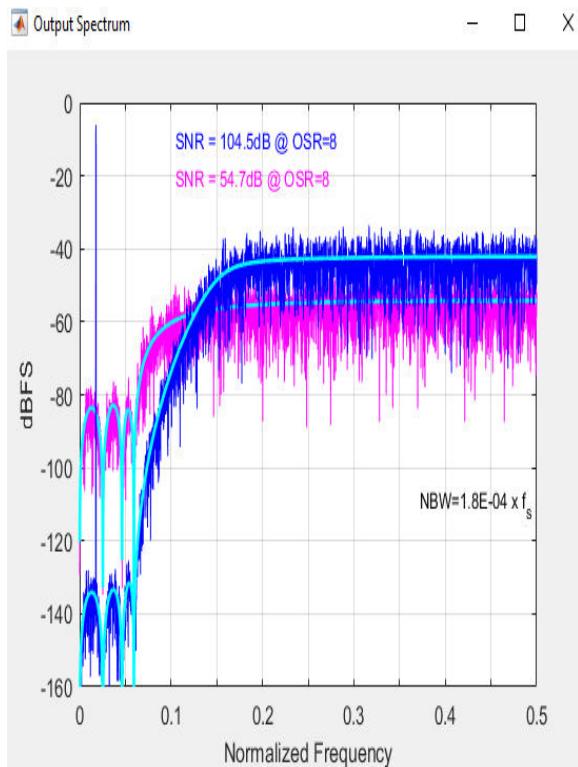


Fig.8 Stability Analysis of 5th Order Filter

The stability can be achieved for high order Sigma Delta Modulator by keeping the gain of Noise Transfer Function to be low. So, low order Sigma Delta Modulator with high OSR can be used for application.

By the use of uniform quantizer, the performance of Sigma Delta Modulator increases drastically. Stability issues can be resolved by using multibit quantizers. But the designing of multibit quantizer is complex. Also its implementation in chip is quite cumbersome, with respect to large scale integration technologies. The stability of loop filter depends upon number of factors like maximum input signal range, position of poles of Noise Transfer Function in unit circle, gain value of the loop filter etc.

So, by considering all the above parameters as per the application, the Sigma Delta Modulator of specific architecture with required order can be used. If the bandwidth requirement is modest, then conventional

model of Sigma Delta Modulator of low order can be used. The Analog to Digital Converters required for audio signals which are having higher bandwidth can use Sigma Delta Modulator of higher order.

CONCLUSION

In this work, analysis of lower order and higher order Sigma Delta Modulator in conjugation with the LMS algorithm has been done on the basis of Signal to Noise Ratio and Effective Number of Bits. The noise shaping property of Sigma Delta Modulator has made it popular in the application where high Signal to Noise Ratio is desired. The significant property of noise shaping, pushes the noise in the range out of band of interest which reduces the requirement of sharp cut off anti aliasing filter. As, the oversampling ratio increases the Signal to Noise Ratio also increases. Higher SNR values can be achieved at lower OSR also, if higher orders of modulators are used. But as the number of integrators in the modulator increases this affects in the position of poles of the Noise Transfer Function which can make the loop filter unstable. It can be concluded from the results and conclusions that the sigma delta scheme is a highly efficient technique that can be utilized for the design of Adaptive Filters which yield low Quantization Noise due to the noise shaping principle employed inherently in the proposed technique.

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